REMARKS

Claims 77–96 are pending in the present application.

Claim 85 was amended.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 103 (Obviousness)

Claims 77–96 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,422,289 to *Pierce et al* in view of U.S. Patent No. 5,346,587 to *Doan et al.* This rejection is respectfully traversed.

Independent claim 77 recites that the source and drain regions each include a first portion in the substrate and a second portion on the substrate over the first portion and adjacent to the insulating material on the sides of the gate electrode. Similarly, independent claim 90 recites that doped regions within the substrate and doped semiconductor material on the substrate form a source and drain for a transistor, while independent claim 96 recites that doped source and drain regions extend into the substrate and within semiconductor material on the substrate. Such a feature is not shown or suggested by the cited references.

Pierce et al discloses in Figure 5 a structure in which the source and drain regions 34 and 36 are completely within the substrate:

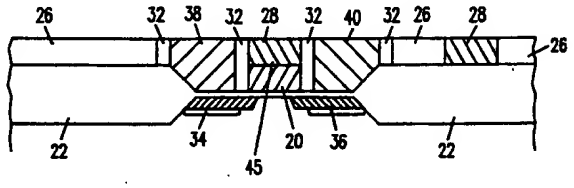

FIG. 5

Conductive contacts or plugs 38 and 40 over the source and drain regions 34 and 36 are provided for electrically contacting source and drain regions 34 and 36. *Pierce et al* teaches that these conductive plugs 38 and 40 may be formed from polysilicon or single crystal silicon doped in situ. *Pierce et al*, column 11, lines 29–46.

As known in the art, MOSFET source and drain regions are the portions of the transistor in which charge carrier generation and recombination occur for the charge carriers which form the current. Saturation current, and therefore transconductance, of the transistor may be constrained by the size of the source and drain regions. Additionally, depletion regions around the source and drain isolate those regions from adjacent semiconductor material of the opposite doping or conductivity type. By convention, the source and drain regions include lightly doped portions beneath the region immediately adjacent the edge of the gate, and perhaps extending under the gate. These lightly doped portions are provided to minimize Miller capacitance between the gate electrode and the source/drain regions, which can slow transistor switching speeds. Heavily doped portions overlap the lightly doped portions at some separation from the

gate electrode, providing sufficient conductivity to reduce overall source/drain resistance and sufficient bulk to support charge carrier generation and recombination, and thus the requisite current. Even the heavily doped portions of source/drain regions, however, are not doped past the point of the material being a semiconductor to form a conductor, as in the case of, for example, doped polysilicon gate electrodes.

In the present invention, the source and drain regions are wrapped around the gate electrode to reduce the area occupied by the transistor. The lightly doped portions may extend into material formed on the substrate to avoid Miller capacitance with the electrode through the insulating sidewalls.

Pierce et al discloses source 34 and drain 36 as formed entirely within the substrate (both the lightly and heavily doped portions) and, in one embodiment, conducting plugs 38 and 40 formed of doped semiconductor material over the source 34 and drain 36. Because the embodiment which employs doped monocrystalline semiconductor material for the plugs 38 and 40 is taught as an equivalent to those in which metal and doped polysilicon are employed for plugs 38 and 40, *Pierce et al* teaches doping of the semiconductor material for plugs 38 and 40 to the point of such material becoming a conductor rather than a semiconductor. As such, plugs 38 and 40 are not part of source and drain regions in which charge carrier generation and recombination occurs.

Pierce et al contains no teaching or suggestion that plugs 38 and 40 are or could be modified to form part of the source/drain regions for the transistor. Moreover, *Pierce et al* teaches that conductive plugs 38 and 40 may be metallic, teaching away from employing raised source/drain regions over the substrate as claimed. *Pierce et al* teaches formation of the transistor structure entirely within the substrate in accordance with the conventional art, with conductive plugs filling the contact openings to planarize the structure. In contrast, the present invention forms a portion of the source/drain regions above the substrate, effectively wrapping the transistor structure around the edges of the gate electrode, allowing a smaller total lateral size for the transistor. *Pierce et al* does not teach or suggest forming the source and drain regions in two portions within and over the substrate.

Claims 87 and 90 recite that the LDD source/drain regions are the first portions of the source and drain, formed within the substrate, as distinct from the second portion. Such a feature is not shown or suggested by the cited references.

Claim 88 recites that the second portions (over the substrate) of the source/drain regions are doped to form heavily doped portions, while claim 91 adds that the first portions (in the substrate) are lightly doped. Such a combination of features is not shown or suggested by the cited references.

Therefore, the rejection of claim 77–96 under 35 U.S.C. § 103 has been overcome.

AMENDMENTS WITH MARKINGS TO SHOW CHANGES MADE

Claim 85 was amended herein as follows:

85. (amended) The integrated circuit structure of claim 77, wherein the first and second portions of the source and drain regions are both formed of a semiconductor material doped to include lightly doped regions and heavily doped regions.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@novakov.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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